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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/956,908	09/21/2001	Yoshiyuki Haraguchi	401378	2662

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EXAMINER	
MEONSKE, TONIA L	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 06/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

PPG

Office Action Summary	Application No.	Applicant(s)	
	09/956,908	HARAGUCHI, YOSHIYUKI	
	Examiner	Art Unit	
	Tonia L Meonske	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *My 10, 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 September 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/10/04, 4/24/03,*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *IDS submitted on 9/21/01*.

DETAILED ACTION

Priority

1. Acknowledgment is made of applicant's claim for foreign priority based on an application filed in the Japan Patent Office on May 11, 2001. It is noted, however, that applicant may not have filed a certified copy of the 2001-3047579 application as required by 35 U.S.C. 119(b) as the copy of the scanned image does not have a copy of a ribbon. Appropriate correction is required.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claim 4 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Specifically Applicant has claimed "a minus relative address may be specified as the relative address". However, how is it possible to skip what has already been executed? The minus value cannot work as described in the system as you can't skip over what you've already executed. How is the system working in a

forward linked list going backward? It appears that a translation error may be causing the disclosed and claimed invention to be unclear. Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claim 1 and 3-5 rejected under 35 U.S.C. 102(b) as being clearly anticipated by Tran et al., US Patent 5, 764,946.

7. Referring to claim 1, Tran et al., have taught a microprocessor comprising:

a. a main memory which stores instructions (Tran et al., column 7, lines 10-14);

b. a queue buffer which pre-fetches and stores instructions from the main memory (Tran et al., column 7, lines 5-33, column 47, lines 39-42);

c. a program counter which generates an address in the main memory in which an instruction to be next executed is stored (Tran et al., column 32, lines 4-27, PC);

d. an instruction decoder which receives and decodes instructions output from the queue buffer (Tran et al., Figure 1, elements 208A-208F); and

e. a queue controller which controls input and output of instructions to the queue buffer based on the address generated and output from the program counter (Tran et al., Figure 17, Prefetch buffer is controlled by the counter and IAD (63:0).), wherein when the instruction decoder recognizes reception of a branch instruction, the instruction decoder processes all the instructions preceding a branch end specified by the branch

instruction as an operand of the branch instruction (Tran et al., column 60, lines 10-17, The preceding instructions to the branch end are voided to NOOP as specified by the branch operand target address, or branch end.), outputs an instruction word length of the branch instruction including the operand to the program counter, thereby updating the address of the program counter (Tran et al., The address of program counter is inherently updated in this manner for each instruction.), and prevents flushing of the queue buffer (Tran et al., column 60, lines 10-17, Instead of flushing the instructions in the buffer, the instructions are treated as NOOP's, thereby preventing flushing of the queue.).

8. Referring to claim 3, Tran et al. have taught the microprocessor according to claim 1, as described above, and wherein a relative address between the branch instruction and branch end is specified to specify the branch end (Tran et al., column 42, line 64-column 43, line 2).

9. Referring to claim 4, Tran et al. have taught the microprocessor according to claim 3, as described above, and wherein the queue controller controls input and output of instructions to the queue buffer so that a plurality of previous instructions, which correspond to a number of relative addresses from the instruction that is currently being executed, remain in the queue buffer (Tran et al., column 42, line 64-column 43, line 2, column 7, lines 5-33, column 47, lines 39-42, Instructions after a branch that are voided to NOOP's remain in the prefetch buffer instead of being flushed out.), and a minus relative address may be specified as the relative address (Tran et al., column 40, line 12-27).

10. Referring to claim 5, tran et al. have taught a microprocessor comprising:

a. a main memory which stores instructions (Tran et al., column 7, lines 10-14);

b. a queue buffer which pre-fetches and stores instructions from the main memory (Tran et al., column 7, lines 5-33, column 47, lines 39-42);

c. a program counter which generates an address in the main memory in which an instruction to be next executed is stored (Tran et al., column 32, lines 4-27, PC);

d. an instruction decoder which receives and decodes instructions output from the queue buffer (Tran et al., Figure 1, elements 208A-208F); and

e. a queue controller which controls input and output of instructions to the queue buffer based on the address generated and output from the program counter (Tran et al., Figure 17, Prefetch buffer is controlled by the counter and IAD (63:0).), wherein when the instruction decoder recognizes reception of a branch instruction, the instruction decoder processes all the instructions preceding a branch end specified by the branch instruction as NOP instructions (Tran et al., column 60, lines 10-17, The preceding instructions to the branch end are voided to NOOP as specified by the branch operand target address, or branch end.), outputs an instruction word length corresponding to the branch instruction and the NOP instructions to the program counter thereby updating the address of the program counter (Tran et al., The address of program counter is inherently updated in this manner for each instruction.), prevents flushing of the queue buffer (Tran et al., column 60, lines 10-17, Instead of flushing the instructions in the buffer, the instructions are treated as NOOP's, thereby preventing flushing of the queue.).

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tran et al., US Patent 5, 764,946 in view of Breeding, Kenneth J., Microprocessor System Design Fundamentals, 1995, Prentice-Hall (Herein after Breeding).

13. Referring to claim 2, Tran et al., have taught the microprocessor according to claim 1, as described above. Tran et al. have not specifically taught wherein a label is used to specify the branch end. However, it is well known in the art that labels are typically used to specify branch ends, or targets, in order to symbolically address the memory, such as the label taught by Breeding (Breeding, page 28, 4th paragraph). Labels are beneficial in order to simplify writing and understanding of the code so that exact addresses are avoided from being calculated and the code can be reused regardless of where the program specifically resides in memory.). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the invention of Tran et al., include a label to specify the branch end, as it is known that labels, such as that taught by Breeding, simplify the writing, understanding, and reusability of the code.

Conclusion

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L Meonske whose telephone number is (703) 305-3993. The examiner can normally be reached on Monday-Friday, 8-4:30.

15. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

16. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

tlm

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100